

Remarks:

Reconsideration of the application, as amended herein, is respectfully requested.

Claims 1 - 4, 6 - 17 and 19 - 30 are presently pending in the application. Claims 1 - 4, 6 - 17, 19 - 23 and 29 - 30 are subject to examination and claims 24 - 28 have been withdrawn from examination. Claim 11 has been amended. New claim 30 has been added.

Applicant gratefully acknowledges that item 5 of the above-identified Office Action indicated that claims 1 - 4, 6 - 10, 16, 17, 19 - 23 and 29 were allowable.

In item 2 of the Office Action, claims 11, 12, 14 and 15 were rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by U. S. Patent No. 6,463,560 to Bhawmik et al ("BHAWMIK").

In item 4 of the Office Action, claim 13 was rejected under 35 U.S.C. § 103(a) as allegedly being obvious over BHAWMIK.

Applicant respectfully traverses the above rejections, as applied to amended claim 11.

More particularly, claim 11 recites, among other limitations:

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a self-test control device for causing testing of the integrated circuit by the self-test device before the integrated circuit is connected to an external testing device that performs a function selected from the group consisting of reading out results of the test and evaluating the results of the test;

a test result memory located on the integrated circuit for storing the results of the test;

an output circuit for forwarding the results stored in said test result memory to the external test device.  
[emphasis added by Applicant]

The amendments to claim 11, as well as new claim 30, are supported by the specification of the instant application, and more particularly, page 15 of the instant application, line 24 - page 16, line 13, which states:

As will be described more precisely later, in response to an external request, the BIST module carries out a test of the components and functions of the integrated circuit that can be tested by it (for example of a memory contained in the integrated circuit) and writes the result of this self test into a test result memory (likewise contained in the integrated circuit). The test result stored in the test result memory is output by the integrated circuit to an external testing device when requested by the latter and is evaluated there. This external testing device in the example considered is a testing device which, in addition to evaluating the results of the self test of the integrated circuit, in addition tests those components or functions of the integrated circuit which cannot be or are not tested by the BIST module, or only partially so, by supplying suitable signals and by evaluating the reaction to these. [emphasis added by Applicant]

As such, among other limitations, Applicant's claim 11 requires that a test be completed on the integrated circuit

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before the integrated circuit is connected to an external testing device, the result being stored in a test result memory on the integrated circuit, and an output device for outputting the results, completed prior to the integrated circuit being connected to an external test device, to an external test device. As such, a test must be completed (i.e., results) prior to the connection of the IC to an external test device and then, once the IC is connected to an external test device, the results of the earlier run test are transferred. Further, Applicant's claim 30, dependent from claim 11, requires the transfer to occur when requested by the external test device.

The BHAWMIK reference fails to teach or suggest, among other limitations of Applicant's claims, performing a test before the IC is connected to an external test device, the results being stored on the IC and forwarded to an external test device. More particularly, BHAWMIK failed to teach or suggest, among other limitations of Applicant's claim 11, running a test on the IC before connection to an external test device, and then, connecting the IC to an external test device, to which the results are transferred.

Rather, the portion of BHAWMIK that was cited in the Office Action disclosed only that a test was after connection to an

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external test device or internally by a BIST circuit, but not by both. For example, col. 1 of BHAWMIK, lines 14 - 23 (cited in the Office Action against Applicant's former claim 11), states:

Integrated circuits (IC) are normally tested both to ensure that the component is defect-free manufactured and/or remains in proper working condition during use. Testing of the IC may for example be accomplished by applying a test pattern to stimulate the inputs of a circuit and monitoring the output response to detect the occurrence of faults. The test patterns may be applied to the circuit using an external testing device. Alternatively, the pattern generator may be a BIST structure comprising part of the internal circuitry of the IC which generates the test patterns. [emphasis added by Applicant]

Clearly, the above-cited portion of BHAWMIK cites the use of an external test device and an internal BIST circuit as alternatives. The above-cited portion of BHAWMIK neither teaches, nor suggests, among other limitations of Applicant's claim 11, testing the integrated circuit before the integrated circuit is connected to an external testing device, the result being stored in a test result memory on the integrated circuit, and an output device for outputting the results, completed prior to the integrated circuit being connected to an external test device, to an external test device. BHAWMIK further does not teach or suggest, among other limitations, of Applicant's claims, transferring the results of the on-board test, completed prior to the integrated circuit being connected to an external test device, to an external test

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device, when requested by the external test device, as  
required by Applicant's new claim 30.

As such, it is believed that Applicant's claims 11 - 15 and 30  
are patentable over the BHAWMIK reference reference. Thus, it  
is believed that all of Applicant's claims are patentable over  
the cited art.

It is accordingly believed that none of the references,  
whether taken alone or in any combination, teach or suggest  
the features of claims 1, 11, 16 and 29. Claims 1, 11, 16 and  
29 are, therefore, believed to be patentable over the art.  
The dependent claims are believed to be patentable as well  
because they all are ultimately dependent on claims 1, 11 and  
16.

In view of the foregoing, reconsideration and allowance of  
claims 1 - 4, 6 - 17 and 19 - 30 are solicited.

In the event the Examiner should still find any of the claims  
to be unpatentable, counsel would appreciate receiving a  
telephone call so that, if possible, patentable language can  
be worked out.

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If an extension of time for this paper is required, petition for extension is herewith made.

It is believed that the addition of claim 30 would not require any further fee, as dependent claims formerly paid for, were previously cancelled. However, please charge any fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner Greenberg Stemer LLP, No. 12-1099.

Respectfully submitted,

  
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